ABSTRACT

After one way of an associative cache is disabled from the perspective of a core processor, a DMA data transfer operation may be commenced to pre-load data into the disabled way from a main memory or to unload data from the disabled way into the main memory. By using a separate decoder for each way of the cache, a few additional multiplexers, and additional control circuitry, different ways of a cache may be accessed concurrently by the core processor and the DMA controller. Therefore, while a DMA transfer operation takes place with respect to the disabled way of the cache, the other ways of the cache remain accessible by the core processor. By properly pre-loading and unloading data from selected ways of the cache in this manner, the cache hit ratio by the core processor can approach 100%.